-REMARKS-

This Amendment is responsive to an Official Action that issued in this case on October 24, 2001. In that Action, the Office finalized a restriction requirement and withdrew claims 11-21 from further consideration in this case. Additionally, the Office objected to the disclosure and the drawings for formal reasons. Furthermore, the Office rejected claims 4-6 and 10 under 35 USC §112, ¶1 and rejected claims 1-10 under 35 USC §103 as being obvious in view of several references.

Responsive to the Action, applicant hereby amends claims 1 and 6, cancels claims 8-21, and adds new claims 22-25. Reconsideration of this case is respectfully requested in view of the foregoing amendments and the following remarks.

Applicant's Invention

As discussed in the Background section of applicant's specification, most state-of-the-art processing technologies produce integrated circuits whose transistors are inherently highly tolerant to damage from ionizing radiation. Although this relatively high radiation tolerance of state-of-the-art integrated circuits is of no benefit to most users and for most applications, it makes these circuits suitable for use in aerospace and military applications. There is a risk, therefore, that these circuits could be used militarily against the United States or its allies. Consequently, Department of Justice export restrictions (ITAR) might prevent those chips from being freely sold or exported. To the extent that a commercial CMOS or NMOS fabricator is restricted by ITAR from freely selling or exporting chips that have a legitimate non-military use, it suffers financially.

Some embodiments of the claimed invention provide integrated circuits that have increased susceptibility to ionizing radiation, but that retain the advantages of contemporary processing technologies (*e.g.*, small feature size, *etc.*). Such integrated circuits can therefore be freely sold and exported without creating the justifiable fear that they can be used militarily against the United States or its allies.

In accordance with the illustrative embodiment of the present invention, an integrated circuit is designed and fabricated with contemporary processing technologies, except that certain devices, referred to in the specification as "safeguard devices," are added to the integrated circuit. The safeguard devices are fabricated so that they, and not the other devices (referred to as "utile devices" in the specification) on the integrated circuit, are susceptible to ionizing radiation. Furthermore, the safeguard devices are coupled into the integrated circuit in such a manner that when the integrated circuit is bombarded with ionizing radiation, the

safeguard devices irreparably destroy (at least in some embodiments) the functionality of the integrated circuit.

In general, the safeguard device can destroy the functionality of an integrated circuit in two ways. First, one or more safeguard devices can interfere with the logical operation of an integrated circuit, by, for example, shorting a signal lead to ground. Second, one or more safeguard devices can interfere with the electrical operation of an integrated circuit by, for example, shorting V_{DD} to ground.

Claim 1, as amended, recites an integrated circuit, comprising:

> a first device comprising a first lead, a second lead, and a third lead, wherein said third lead of said first device is electrically connected to ground; and
>
> a second device comprising a first lead, a second lead, and a third lead, wherein said third lead of said second device is electrically connected to ground, and wherein said first lead of said second device is electrically connected to said first lead of said first device;
>
> wherein the effective threshold voltage of said first device is more susceptible to be lowered by ionizing radiation than is the effective threshold voltage of said second device.

The limitation that recites that the effective threshold voltage of the first device is more susceptible to be lowered by ionizing radiation than is the effective threshold voltage of the second device indicates that the first device functions as a "safeguard device" and the second device is a "utile device."

The clause pertaining to the "second device" includes a limitation that:

> said first lead of said second device is electrically connected to said first lead of said first device ...

This electrical connection between the first device and the second device, as recited in amended claim 1, enables the first device to affect the operation of the second device (*e.g.*, irreparably damaging the integrated circuit, *etc.*) and, indeed, the whole circuit.

The Claims are Allowable
Over the Art of Record

The Office rejected claims 1-10 over U.S. Pat. No. 5,589,708 to Kalnitsky or U.S. Pat. No. 5,748,412 to Murdock et al. These patents neither disclose nor suggest applicant's claimed invention.

Kalnitsky discloses radiation hard integrated circuits in which silicon has been implanted in the gate oxide layer, field oxide region and the inter-level dielectric layer. Kalnitsky states that implanting silicon ions in this fashion forms electron traps that capture radiation-induced electrons, thereby increasing the radiation hardness of the circuit.

Kalnitsky discloses that by using this implantation technique, a "dosimeter" can be created within an integrated circuit. In particular, Kalnitsky discloses that radiation hard transistors as well as standard transistors can be formed on the same integrated circuit. This is done by selectively doping different portions of a circuit. According to Kalnitsky, the two different types of transistors will degrade or recover from the ionizing radiation at different rates. Consequently, Kalnitsky proposes locating a sensor on the chip that can determine any differences between the performance of the two types of transistors, thereby sensing the accumulated radiation dose. According to Kalnitsky, a "self-adapting" circuit that responds to the sensor could be used to compensate for loss in performance due to the ionizing radiation.

As an initial matter, Kalnitsky, fairly read, teaches away from the claimed invention. Although perhaps an over-used argument for rebutting an obvious rejection, it seems to be apropos in this case. In particular:

- While applicant modifies fabrication procedures to produce dose *soft* (reduced radiation resistance) circuit elements, Kalnitsky modifies procedures to produce dose *hard* (enhanced radiation resistance) transistors.
- While applicant produces dose soft circuit elements to sabotage and, in some case, irreparably damage the operation of an integrated circuit on exposure to ionizing radiation, Kalnitsky produces dose hard circuit elements to keep an integrated circuit properly functioning (*i.e.*, include a sensor and a self-adapting circuit to compensate for loss of performance).

Kalnitsky does not disclose the claimed limitation (amended claim 1) that two devices having different radiation susceptibility (*e.g.*, two different types of transistors, *etc.*) are electrically connected. And clearly, there is no suggestion in Kalnitsky to do so. Kalnitsky discloses sensing the difference in performance between the two types of transistors; consequently, these transistors should not be electrically connected to one another.

Since Kalnitsky does not disclose or suggest a limitation that is recited in amended claim 1, that claim is allowable over Kalnitsky. Claims 2-7 are likewise allowable since they are dependent upon claim 1, in addition to reciting additional patentable features.

Murdock discloses a method and apparatus for protecting magnetoresistive sensor elements from electrostatic discharge. The apparatus includes a magnetoresistive sensor, detection circuitry, and "reader" conductors that are located between the two. A diode assembly interconnects the reader conductors. The diode assembly incorporates "soft" diodes that might conduct at a voltage that is less than the operating voltage of the magnetoresistive sensor. The diode assembly has a resistance that prevents electrical conduction across the diode assembly between the reader conductors when the voltage between the reader conductors is less than or equal to an operating voltage of the magnetoresistive sensor. When the voltage between the reader conductors is greater than a pre-selected protection voltage threshold (based on the sensivity of the magnetoresistive sensor to electrostatic discharge), the diode assembly shunts current across the diode assembly between the reader conductors thereby "short circuiting" the reader conductors.

Applicant's invention pertains to ionizing radiation, which is high-energy radiation that is capable of producing ionization in substances through which it passes. Ionizing radiation includes highly-energetic charged particles such as alpha and beta rays, and non-particulate radiation such as x-rays and neutrons. Murdock does not pertain to ionizing radiation; it pertains to electrostatic discharge. Electrostatic discharge is a transient movement of charges that were at rest.

In Murdock, the soft diodes do not need to be exposed to ionizing radiation, or any causative agent, to conduct at a low voltage—they are made to conduct at low voltage. In applicant's invention, the safeguard devices (*e.g.*, radiation-soft transistors) behave normally until exposed to a certain level of radiation.

Furthermore, like Kalnitsky, Murdock teaches *protecting* a circuit (*i.e.*, the magnetoresistive sensor) when exposed to an undesirable condition (*i.e.*, high voltage). Applicant teaches, at least in some embodiments, *destroying* a circuit when exposed to an undesirable condition (*i.e.*, a certain level of ionizing radiation). While such destruction is not recited, *per se*, in claim 1, this and the other differences identified above do speak to the issue of the obviousness — that is, the extent to which Murdock is "suggestive" of any features of claimed invention. Clearly, Murdock is not suggestive of the claimed invention.

Murdock does not disclose the claimed limitation (claim 1) that:

> the effective threshold voltage of said first device is more susceptible to be lowered by ionizing radiation than is the effective threshold voltage of said second device.

Since Murdock does not disclose or suggest a limitation that is recited in amended claim 1, that claim is allowable over Murdock. Claims 2-7 are likewise allowable since they are dependent upon claim 1, in addition to reciting additional patentable features.

The Rejection of Claims 4-6 under 35 USC §112, ¶1 Should be Withdrawn

The Office alleged that claims 4-6 and 10 contain subject matter that was not described in the specification in such a way as to enable one skilled in the art to make or use the invention. In particular, as to claims 4-5 and 10, the Office alleged that there is "no adequate description ... for an integrated circuit compris[ing] a microprocessor that comprises a control sequencer coupled to an arithmetic logic unit, and an integrated circuit compris[ing] an arrangement of memory cells operatively coupled to an address decoder." Applicant respectfully disagrees.

Those skilled in the art know how to make an integrated circuit that comprises a microprocessor having a control sequencer coupled to an arithmetic logic unit. Similarly, those skilled in the art know how to make an integrated circuit that comprises an arrangement of memory cells operatively coupled to an address decoder

The illustrative embodiment of Applicant's invention is, as already described, to combine utile devices and safeguard devices in a circuit in such a way that if levels of ionizing radiation exceed a certain dose, the circuit will fail. The microprocessor, control sequencer, arithmetic logic unit, memory cells and address decoder, as recited in claims 4, 5 and 10 are simply specific examples of some utile devices:

> a "utile device" is define as a device that processes an information-bearing signal.... Typically, the utile devices on an integrated circuit provide the functionality for which the circuit was designed and fabricated and utilized. [T]he utile devices on an integrated circuit might function as **a microprocessor with a control sequencer and an arithmetic logic unit, a plurality of memory cells, an amplifier, *etc.***

(Page 8, lines 3-8, emphasis added.) Applicant describes the manner of connecting the various utile and safeguard devices to create integrated circuits in accordance with the present invention.

As to utile devices:

> As shown in FIG. 2, utile devices typically have: (i) input signals, which might be received from off of integrated circuit 200 or that might be generated by other utile devices, and (ii) output signals, which might be sent off of integrated circuit 200 or might be fed into other utile devices. It will be clear to those skilled in the art how to make and use one or more utile devices in accordance with the illustrative embodiment of the present invention.
>
> Electrical conductor 211 and electrical conductor 212 can be metal bus lines or specific transistor diffusion nodes, as are well-known in the art, and it will be clear to those skilled in the art how to make and use electrical conductor 211 and electrical conductor 212 in conjunction with utile devices 201-1 through 201-*N*. It is well-known to those skilled in the art how to make and use integrated circuit 200.

(Page 8, lines 9-19.) As to safeguard devices (page 9, lines 5-13)::

> The details of a safeguard device are discussed with respect to FIG. 4 below. Although one lead of a safeguard device is always tied to ground, the other lead can be either connected to power (*i.e.*, V_{DD}) or to a signal lead (*e.g.*, signal lead 313-*i*, *etc.*). The theory of operation of the illustrative embodiment is as follows: when integrated circuit 300 is exposed to ionizing radiation, a safeguard device shorts its two terminals together. When the safeguard device is connected between power and ground, the safeguard device shorts power to ground. When the safeguard device is connected between the signal lead and ground, the safeguard device shorts the signal lead to ground. In either case, the integrated circuit is affected.

It is submitted, therefore, that the specification provides adequate description for claims 4, 5 and 10. Consequently, it is requested that Office withdraw the rejection of claims 4 and 5 under 35 USC §112, ¶1 (claim 10 is now cancelled).

The rejection of claim 6, on the other hand, was appropriate. That claim previously recited, in pertinent part, that:

> said **third** lead of said first device is connected to power, and said **third** lead of said second device is connected to power.

This claim, in fact, is inconsistent with claim 1, which recites that the third lead of both the first device and the second device are connected to ground. The applicant had intended claim 6 to read:

> said **first** lead of said first device is connected to power, and said **first** lead of said second device is connected to power.

Claim 6 has been so amended. The amendment to claim 6 is supported by the drawings and the description. Consequently, it is requested that Office withdraw the rejection of claim 6 under 35 USC §112, ¶1.

All Structural Detail that is
Essential for a Proper
Understanding of the Invention
is Shown in the Drawings

The Office objected to the Drawings alleging that they fail to show "FOX region including high concentration of positive charge trapping centers as described in the specification."

Applicant assumes that by the term "FOX," the Office is referring to the "field oxide" region of a transistor. It is known to those skilled in the art that electron-hole pairs are generated in the gate dielectric and field oxide region on exposure to ionizing radiation. Some of the holes become trapped in the gate dielectric and the field oxide region as various gate-induced fields sweep out the electrons as part of normal circuit operation. Because the holes behave like positive charge, this phenomenon is referred to as positive charge trapping.

FIGS. 1A-1C show the various oxide regions, including the gate dielectric, the field oxide, *etc.* FIG. 1C shows that the field oxide (112) is substantially thicker than the gate dielectric (118). The field oxide traps more positive charge than the gate dielectric because it is thicker than the gate dielectric. Since the phenomenon of positive charge trapping is known to those skilled in the art, it is submitted that indicating, in the drawings, a higher concentration of holes in the relatively thicker field oxide region (112) than the relatively thinner gate dielectric (118) is not essential to a proper understanding of the invention. Such understanding can be obtained from reading the specification and viewing the drawings as filed.

Consequently, the Office is requested to withdraw its objection to the drawings.

New Claims 22-25
are Allowable

New claim 22 recites the limitation that:

> upon exposure to a sufficient amount of ionizing radiation, said safeguard device turns on before said utile device, and affects operation of said utile device.

This feature is not discloses or suggest by the art of record, so that claim 22 is allowable. Claims 23-25 are allowable based upon their dependence upon claim 22, in addition to reciting further patentable features.

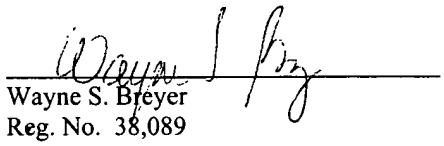
Support for new claim 22 appears in the specification at, *e.g.*, page 10, lines 29+. Support for new claims 23-24 appears in the specification at, *e.g.*, page 9, lines 5-12. Claim 25 has previously been presented (although dependent upon a different base claim; *see* claim 2).

Conclusion

It is believed that claims 1-8 now presented for examination are allowable. A notice to that effect is solicited.

Respectfully,

DeMont & Breyer, LLC



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-Amendments Showing Changes Made-

IN THE SPECIFICATION:

1. "Apparatus and Method for Manufacturing a Semiconductor Circuit," Serial No., 09/**590,809, filed June 9, 2000** [___,___, (Attorney Docket 280-1/FE-00444)];
2. "Semiconductor Device and Circuit Having Low Tolerance to Ionizing Radiation," Serial No., 09/**590,806, filed June 9, 2000** [___,___, (Attorney Docket 280-2/FE-00443)]; and
3. "Semiconductor Circuit Having Increased Susceptibility to Ionizing Radiation," Serial No., 09/**592,473, file June 9, 2000** [___,___, (Attorney Docket 280-4/FE-00442)].

IN THE CLAIMS

1. (Amended) An integrated circuit comprising:

a first device comprising a first lead, a second lead, and a third lead, wherein said third lead of said first device is electrically connected to ground; and

a second device comprising a first lead, a second lead, and a third lead, wherein said third lead of said second device is electrically connected to ground**, and wherein said first lead of said second device is electrically connected to said first lead of said first device**;

wherein the effective threshold voltage of said first device is more susceptible to be lowered by ionizing radiation than is the effective threshold voltage of said second device.

6. (Amended) The integrated circuit of claim 1 wherein said second lead of said first device is connected to ground, said **first** [third] lead of said first device is connected to power, and said **first** [third] lead of said second device is connected to power.